



IMAGE SENSOR FABRICATION METHOD AND STRUCTURE

[0001] This application is a continuation in part of U.S. Patent Application No. 10/456,759, filed June 6, 2003.

FIELD OF THE INVENTION

5 [0002] The present invention relates to semiconductor devices generally, and more specifically to solid-state color filters.

BACKGROUND

[0003] Color filters suitable for use in color image sensors have been described in U.S. Patents Nos. 6171885, 6395576, 6274917, 6482669 and 6495813, all of which are incorporated
10 by reference herein in their entireties.

[0004] A color image sensor is typically a charge-coupled device (CCD) or complementary metal-oxide semiconductor (CMOS) photodiode array structure. The structure includes a spectrally photosensitive layer below one or more layers patterned in an array of color filters, above which resides a surface-layer array of microlens elements. In some conventional
15 configurations, a color pixel is formed using four adjacent pixels on an image sensor. Each of the four pixels is covered by a different color filter selected from the group of red, blue and two green pixels, thereby exposing each monochromatic pixel to only one of the three basic colors. Simple algorithms are subsequently applied to merge the inputs from the three monochromatic pixels to form one full color pixel.

20 [0005] FIGS. 1A and 1B show color filters having the "stripe defect." The stripe defect occurs when one of the color resist layers is thicker or thinner than the nominal value. In FIG. 1A, the stripe defect is due to a difference between the thicknesses of the blue and green resist. The sensor 100 includes a plurality of scribe lines 120 arranged in a rectangular array. A plurality of filter regions are surrounded by the scribe lines 120. The filter regions include active
25 regions 110 and bond pad regions 130 arranged within the scribe lines 120. The stripe defect is indicated by the plurality of regions, designated "B", in which either the blue resist layer is thicker than its nominal value, or the green resist layer is thinner than its nominal value, and a plurality of regions designated "G" in which either the green resist layer is thicker than its

nominal value, or the blue resist layer is thinner than its nominal value. Similarly, in FIG. 1B, the defect is due to a difference between the thicknesses of the green and red resist. In FIG. 1B, active regions are 110', bond pad regions are 130' and scribe lines are 120'. In regions designated "G", either the green resist layer is thicker than its nominal value, or the red resist layer is thinner than its nominal value. In regions designated "R", either the red resist layer is thicker than its nominal value, or the green resist layer is thinner than its nominal value.

[0006] FIG. 1C is a side cross sectional view of a conventional CMOS imaging sensor (CIS) 100. The CIS 100 has a substrate 107 having a plurality of scribe lines 109 arranged to form at least one filter region 101 surrounded by the scribe lines. The substrate 107 may be an insulating substrate, or an insulating layer (e.g., SiO₂) above a semiconductor substrate. In a wafer having many filter regions 101, the plurality of scribe lines 109 form a grid of perpendicular lines. The filter region 101 includes an active region 102 and a bond pad region 108 with bond pads 122 thereon. The active region 102 may have n- or p+ well photo diodes therein, and may be, for example polycrystalline silicon. Active region 102 has a passivation layer 114 (e.g., SiN) thereon. The passivation layer 114 has a plurality of top metal regions 103. The passivation layer 114 has a planarization layer 104a formed thereon, which may be a resist layer thicker than the height of the steps on the wafer surface. Planarization layer 104a can be cast on the wafer and can be planarized by, for example, a free viscous flow of the resist at an elevated baking temperature or by a forced resist flow through pressing a flat mold on the resist surface while heating. Above the first planarization layer 104a, blue, green and red color resist layers are formed, designated 111 and 113. A second planar layer 104b is above the filters 111 and 113. A microlens layer 106 is formed above the second planar layer 104b.

[0007] The height 119 of layer 104b relative to the top of the passivation layer 114 may be about 4.5 μm . There is an additional height 118 of about 1.5 μm to 2 μm between the top of bond pad 122 and the top of the passivation layer 114, so the total step height between the top of passivation layer 114 and the top of the bond pad 122 is about 6 μm to 6.5 μm .

[0008] If the color filter signal deviation is too large, CMOS image sensor performance may be affected, resulting in yield loss as high as 15 to 20%. For example, the inventors of this application are aware of product samples in which the observed color signal standard deviations were: blue 3.93%, green 2.84% and red 1.68%. This corresponds to a yield measure Cpk of lower than 0.5.

[0009] The color filter deposition process and its relationship to the microlens array formation process are known to influence the production cycle-time, test-time, yield, and ultimate manufacturing cost.

[0010] A method of making a color filter with less signal deviation and improved yield is
5 desired.

SUMMARY OF THE INVENTION

[0011] A method for processing a semiconductor substrate comprises the steps of:
providing a substrate having at least one filter region with a plurality of bond pads therein,
depositing metal above the bond pads, to reduce a step height thereof, forming a planarization
10 layer such that the deposited metal has a height near to a height of the planarization layer, and
forming the at least one color resist layer above the planarization layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIG. 1 is a plan view showing a plurality of color filter active regions that exhibit the stripe defect.

15 [0013] FIG. 1C is a cross sectional view showing a conventional color image sensor.

[0014] FIG. 2 is a cross sectional view showing an active region of a color image sensor formed using an exemplary method.

[0015] FIG. 3 is a plan view of a mask over the substrate shown in FIG. 2.

[0016] FIG. 4 is a cross sectional view showing an active region of a color image sensor
20 formed processed using a different mask.

[0017] FIG. 5 is a plan view of a mask used to deposit resist on the color image sensor shown in FIG. 4.

[0018] FIGS. 6 to 9 show another exemplary embodiment of a method for fabricating a color image sensor.

25 DETAILED DESCRIPTION

[0019] U.S. Patent Application No. 10/456,759, filed June 6, 2003, is incorporated by reference in its entirety, as though set forth fully herein.

[0020] This description of the exemplary embodiments is intended to be read in connection with the accompanying drawings, which are to be considered part of the entire written description. In the description, relative terms such as "lower," "upper," "horizontal," "vertical," "above," "below," "up," "down," "top" and "bottom" as well as derivative thereof (e.g., "horizontally," "downwardly," "upwardly," etc.) should be construed to refer to the orientation as then described or as shown in the drawing under discussion. These relative terms are for convenience of description and do not require that the apparatus be constructed or operated in a particular orientation. In the drawings, like reference numerals indicate like components or items.

10 [0021] The inventors have determined that a major factor in causing color signal deviation in color filters is a problem referred to herein as the "stripe defect." The stripe defect refers to a condition in which the thickness of the color resist layers is not uniform within and/or between pixels. This is especially a problem with blue and green color resist layers. When the active region is viewed from above, these non-uniform color resist layers appear to have blue and green stripes or irregular regions.

15 [0022] The inventors have determined that the stripe defect is caused by serious front end topography issues. That is, the front end of the processing flow leaves an uneven surface on the semiconductor substrate on which the color filters are formed. This uneven surface degrades the ability to deposit planar layers above it.

20 [0023] The inventors have further determined that the deeper the step height of the scribe lines in the substrate, the more serious the stripe defect becomes. A secondary factor is the step height of the bond pad. Additional factors include the photoresist coating speed; higher coating speeds increase the stripe defect. However, the scribe line step height is the major cause of the stripe defect, and the bond pad step height is the next most significant factor.

25 [0024] FIG. 2 is a cross-sectional view of an exemplary color filter device 200. The device 200 has a substrate having a plurality of scribe lines 210 arranged to form at least one filter region 201 surrounded by the scribe lines 210. The substrate 207 may be an insulating substrate, or an insulating layer (e.g., SiO₂) above a semiconductor substrate. In a wafer having many filter regions 201, the plurality of scribe lines 210 form a grid of perpendicular lines. The filter region 30 201 includes an active region 202 and a bond pad region 208 with bond pads 222 thereon. The active region 202 may have n- or p+ well photo diodes therein, and may be, for example

polycrystalline silicon. The active region 202 has a passivation layer 214 (e.g., SiN) thereon. The passivation layer 214 has a plurality of top metal regions 203. The passivation layer 214 has a planarization layer 204a formed thereon, which may be a resist layer thicker than the height of the steps on the wafer surface. Preferably, planarization layer 204a is formed of a photoresist having high sensitivity and transmittance. Planarization layer 204a can be cast on the wafer and can be planarized by, for example, a free viscous flow of the resist at an elevated baking temperature or by a forced resist flow through pressing a flat mold on the resist surface while heating.

[0025] Above the first planarization layer 204a, blue, green and red color resist layers are formed, designated 211 and 213. The red color resist is not shown in FIG. 2, due to the arrangement of the red, green and blue color resist, but one of ordinary skill understands that when viewed from above, the color resist is arranged with groups of four green resist elements arranged in diamond configurations, with either a red or a blue resist element at the center of each diamond. Another sectional view (not shown) through the same device would show only green and red resist elements. A second planar layer 204b is above the filters 211 and 213. A microlens layer 206 is formed above the second planar layer 204b.

[0026] The scribe lines 210 initially have a step height H. The step height H depends on the type of integrated circuit (IC) technology. For example, a 0.6 μm CMOS image sensor has a scribe line step height H of 3.33 μm . A 0.35 μm CMOS image sensor has a scribe line step height H of 4.55 μm . A 0.25 μm CMOS image sensor has a scribe line step height H deeper than 4.55 μm . Other IC technologies will have corresponding step heights H which may differ from these.

[0027] In the exemplary embodiments, the step of depositing the planarization layer 204a is modified to include at least partially filling the scribe lines 210 with a resist material 212 to reduce the step height of the scribe lines to H2 (where the step height H2 after the partial filling is the distance between the surface of the resist and the surface of the substrate). By at least partially filling the scribe line with resist, the uneven topography is reduced or eliminated, allowing uniform formation of the color resist layers 211 and 213.

[0028] In FIG. 2, the resist 212 is only deposited inside the scribe line 210 to partially fill the scribe line 210. In some embodiments, the at least partial filling of the scribe line with resist is completed with the top of the resist below the surface of the substrate (i.e., with a positive step

height remaining). In other embodiments, the scribe line 210 is completely filled, as described further below.

[0029] FIG. 3 shows an example of a mask that can be used to deposit the resist 212 in FIG. 2. In some embodiments, the mask is clear in the scribe lines 210 and dark outside of the scribe lines (for a negative resist). The resist in the scribe line regions becomes insoluble (hardened) upon exposure to the radiation, and the resist outside of the scribe lines remains soluble, for removal.

[0030] In other embodiments, the mask pattern is reversed, and the mask causes a positive photoresist outside the scribe line region to become soluble, in order keep resist in the scribe line 210 only. The mask is clear outside of the scribe lines and dark inside the scribe lines (for a positive resist). The resist inside the scribe lines remains insoluble and is kept.

[0031] In some embodiments, a chemical solution is applied to dissolve and remove the soluble portion of the resist outside the scribe lines 210. In other embodiments, dry plasma etch is used, where ions energized by a plasma field hit the portion of resist layer outside the scribe lines 210 and chemically dissolve it. The resist 212 remains in the scribe lines 210.

[0032] FIG. 4 is another example of a color filter 300, in which the resist 412 completely fills the scribe line, and continues above the substrate to about the height of the planarization layer 204a. In FIG. 4, the resist 412 is deposited all across the substrate, except in the immediate vicinity of the bond pads 222. This allows a greater degree of planarization, and is believed to promote formation of color resist layers 211 and 213 with more uniform thickness.

[0033] FIG. 5 shows a mask 400 that can be used to perform the photoresist deposition step for depositing the resist 412 of FIG. 4. The exemplary mask 400 is clear throughout (assuming a negative resist is used), except within the square regions 302, which overlie the bond pad regions 208 and surround the bond pads 222. The mask is dark in regions 302. As a result, when the substrate is exposed through the mask 400, the resist is exposed everywhere except in the bond pad regions 302. After exposure, the portion of resist layer outside of the bond pad regions 302 becomes insoluble. The soluble portion of the resist in the bond pad regions 302 is removed using, for example, a chemical solution or dry plasma etch as described above, and the resist 412 remains in the scribe lines 210.

[0034] In other embodiments, (where a positive resist is used) the mask pattern is reversed, so that only the bond pad regions are exposed, and the exposed portion of resist layer becomes

soluble. The portions of the resist outside the bond pad regions (including the resist in the scribe lines) remains insoluble.

[0035] The resist material 212, 412 may include any energy-sensitive material that can be formed on a substrate to create a pattern during integrated circuit manufacturing. Resist material 212 may contain, among many other ingredients, energy-sensitive polymers which change from soluble to insoluble after exposure to an energy source for a negative resist; and vice versa for positive resist. Resist material generally is tailored to a specific exposure source. In some embodiments, 248 nm resist material for deep ultraviolet (UV) at 248 nm or 193 nm resist material for deep ultraviolet (DUV) at 193 nm is employed. These are only examples, and other resists (including UV, DUV, X-ray and e-beam resists) may be used.

[0036] In some embodiments, the resist 412 is planarized, using a process such as etching. In some embodiments, the steps of applying the resist 412 and etching back the resist (to planarize the resist) are repeated a plurality of times, until a desired degree of planarization is achieved, and the step height in the scribe line is reduced to a desired amount.

[0037] In some embodiments, a mask such as that shown in FIG. 3 is used through one or more iterations to deposit photoresist in the scribe lines, followed by deposition using a mask such as that shown in FIG. 5 to deposit the resist above the surface of the substrate 207.

[0038] After the resist material 412 is deposited, a regular planarization mask (not shown) may be used to deposit photoresist on the active region 202 within the filter region, to form the planarization layer 204a. At least one color resist layer 211, 213 is formed above the substrate within the at least one filter region while the hardened (insoluble) resist material remains in the scribe lines. Then the second planarization layer 204b is formed, and the microlens layer 206 is formed.

[0039] Once the resist 412 is deposited in the scribe line 210, the resist can be kept in the scribe lines permanently (i.e., until dicing). The presence of the resist in the scribe lines does not interfere with subsequent processing operations (such as dicing), and does not interfere in any way with device performance. The resist 412 may optionally be removed from the scribe lines, if desired.

[0040] In an experiment, a 0.35 μm CMOS image sensor was formed. Prior to depositing the resist 412, the scribe line step height was 4.55 μm . After depositing a first layer of the resist using the mask shown in FIG. 5, the step height (i.e., the distance from the top of the resist to the

top of the substrate) was reduced to 2.6 μm , a 43% reduction. After depositing a second layer of resist using the same mask, the step height was reduced to 0.6 μm . This represents an 87% reduction in the step height. The experiment showed that the yield (as measured by Cpk) greatly improved. Table 1 provides the results in terms of color non-uniformity. In Table 1, the 001A mask refers to a conventional mask used to form a planarization layer 204a in the active region. The 001B mask refers to the mask shown in FIG. 5. Thus, the columns designated "1X 001A mask only" refers to a conventional process. The mean and standard deviation refer to the color filter signal deviations.

Table 1

Color	1X 001A mask only			1X 001B mask combined with 001A			2X 001B mask combined with 001A		
	Mean	Std dev.	Cpk	Mean	Std dev.	Cpk	Mean	Std dev.	Cpk
Blue	8.49%	3.93%	-0.08	5.16%	0.93%	0.84%	4.38%	0.53%	1.96
Green	6.45%	2.84%	0.12	X	X	X	4.13%	0.45%	2.5
Red	5.32%	1.68%	0.43	X	X	X	4.34%	0.51%	2.07

[0041] In Table 1, the columns designated, "1X 001B mask combined with 001A," refers to a process in which the mask 001B shown in FIG. 5 is used to deposit one layer of resist in the scribe lines (partially filling the scribe line), followed by deposition of the planarization layer 204a on the active region 202. The columns designated, "2X 001B mask combined with 001A," refers to a process in which the mask 001B shown in FIG. 5 is used to deposit two layers of resist in the scribe lines (partially filling the scribe line), followed by deposition of the planarization layer 204a on the active region 202. As a reference, a Cpk value of 0.5 corresponds to a yield of about 85%, and a Cpk value of 1.9 corresponds to a yield value near 100%.

[0042] Thus, by partially or completely filling the scribe line with resist before forming the color filter layer 211, 213, a more planar surface is provided, enhancing the uniformity of the subsequently formed color filter layers.

[0043] Although an example is describe above in which two depositions of resist are used, any desired number of resist depositions may be used, depending on the depth of the scribe lines.

[0044] FIG. 9 is a cross sectional view showing another exemplary embodiment, in which the step height of the bond pad 222 is reduced, in addition to reducing the step height of the scribe line. Fabrication of the CIS is shown in FIGS. 6-9.

[0045] Referring first to FIG. 6, fabrication of the CIS begins with formation of the insulation layer 207, deposition and doping of the semiconductor (e.g., polycrystalline silicon) layer 205, deposition of the bottom passivation layer 214, and deposition of the layer for top metal 203 and bond pad 222, which may be aluminum/copper, for example. The top passivation layer 214 is then deposited and etched, to expose the bond pad 222. The step height 218 between the top of the bond pad 222 and the top of the passivation layer 214 may be about 1.5 μm to 2 μm at this point. As noted above, when the planarization layers 204a and 204b are added, the step height could grow to between about 6 μm and 6.5 μm , if no action is taken to reduce the step height.

[0046] As shown in FIG. 6, an added step includes depositing a post-passivation pad portion 224 on top of the bond pad 222, to form a bond pad structure (including bond pad 222 and portion 224) having a height greater than the height of the bond pad, and having a step height less than that of the bond pad. The post-passivation pad portion 224 is formed of the same material as the bond pad 222, using a process such as sputtering, a lithographic process, or photoresist etching (stripping). The thickness of the post-passivation pad portion 224 may be from about 1.5 μm to about 6.0 μm , depending on the step height to be reduced or eliminated.

[0047] FIG. 7 shows the structure of FIG. 6, after a planarization layer 204a is deposited. Preferably, planarization layer 204a has high sensitivity and transmittance. In some embodiments, the material (e.g., photoresist) of planarization layer 204a fills the scribe line 210, in the manner described above with reference to FIG. 4, as indicated by reference numeral 412. Preferably, the material 412 remains in the scribe line until the dicing step. In the embodiment of FIG. 7, only the post-passivation pad portion 224 is exposed.

[0048] Preferably, the top of the post-passivation pad portion 224 is (exactly or) approximately as high as the top of the planarization layer 204a (resulting in approximately zero step height between the pad portion 224 and the planarization layer 204a). Some improvement in yield can be obtained with a smaller height for post-passivation pad portion 224 (resulting in a reduced, but non-zero step height), but the improvement is greater with the height of the post-passivation pad portion 224 approximately as high as the top of the planarization layer 204a. In FIG. 7, the post-passivation pad portion 224 is slightly higher than the top of the planarization layer 204a. The resulting structure shown in FIG. 7 has a planar topography, which is advantageous for reducing the stripe defect in the color photoresist layers 211, 213.

[0049] In other embodiments (not shown), the post-passivation pad portion 224 is provided, and the planarization layer 204a above the active region 202 has approximately zero step height relative to pad portion 224, but the scribe line 210 is not filled with the planarization material. Although such embodiments provide a yield improvement relative to the prior art structure of FIG. 1C, the yield improvement is greater when the material 412 also fills the scribe line as shown in FIG. 7.

[0050] FIG. 8 shows the steps of forming the color filter layers 211, 213 and the spacer layer 204b. The spacer layer 204b is formed of the same material as the planarization layer 204a, and completely covers the color filter layer(s) 211, 213. In preferred embodiments, the spacer layer 204b also covers the scribe line, so that only the post-passivation pad portion 224 is exposed. The resulting configuration shown in FIG. 8 has a planar top surface, which is advantageous for reducing the stripe defect in the microlenses 206. The step height between the top of spacer 204b and the post-passivation pad portion 224 is substantially less than the sum of height 118 and height 119 between top of spacer 104b and the bond pad 122 ($4.5\text{ }\mu\text{m} + [1.5\text{ }\mu\text{m to } 2\text{ }\mu\text{m}] = 6\text{ }\mu\text{m to } 6.5\text{ }\mu\text{m}$) shown in FIG. 1C.

[0051] FIG. 9 show the configuration after formation of the microlenses 206. Following formation of the microlenses, heat is applied and the microlens material is reflowed.

[0052] Although the invention has been described in terms of exemplary embodiments, it is not limited thereto. Rather, the appended claims should be construed broadly, to include other variants and embodiments of the invention, which may be made by those skilled in the art without departing from the scope and range of equivalents of the invention.